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Chung-Ho Chen; Feng-Fu Lin;
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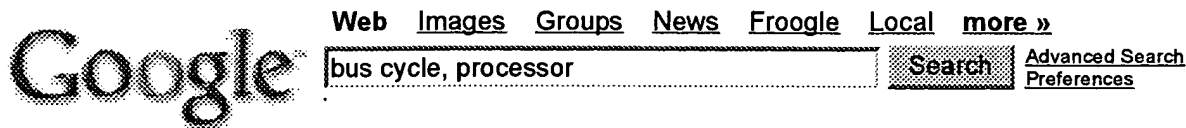Volume 3, 16-20 Feb. 2004 Page(s):318 - 323 Vol.3

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Here's the 10 minute introduction to **bus cycles**, so you can at least look ... The biggest
difference is that during a Write **cycle** the **processor** drives ...
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TLA family **processor** and **bus** supports provide you with an easy-to-use acquisition ... This
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Patent 5701422: Method for ensuring **cycle** ordering requirements ...
3, **processor** 212 gains ownership of node **bus** 230 and initiates a read request ... A write
to this line will cause a write-through **cycle** to the memory **bus**. ...
www.freepatentsonline.com/5701422.html - 46k - Cached - Similar pages

Patent 5163143: Enhanced locked **bus cycle** control in a cache ...
a. in mode one all **processor bus** lock **cycle** signals are passed to said cache memory ... A
method of controlling **processor** locked **bus cycle** operation of a ...
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PDP11/20
18 bit memory address; RUN - **processor** running; **BUS** - **bus** busy; FETCH - instruction
fetch **bus cycle**; EXEC - instruction execute phase; 16 bit data display ...
www.psych.usyd.edu.au/pdp-11/11_20.html - 5k - Cached - Similar pages

Direct Memory Access (DMA)
During any given **bus cycle**, one of the system components connected to the system
bus ... The DMAC effectively steals **cycles** from the **processor** in order to ...
www.electronics.dit.ie/staff/tscarff/DMA/dma.htm - 8k - Cached - Similar pages

Power Management Features On The Embedded Ultra Low-Power Intel486 ...
The **processor** will issue a normal HALT **bus cycle** when entering this state. ... If this
occurs, the **processor** will generate a Stop Grant **bus cycle** and enter ...
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instruction **cycle processor** accesses memory at least once ...
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